Notice of Allowability	Application No.	Applicant(s)	
	10/658,036	GRECO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt of 2/8/05*.

2. ☒ The allowed claim(s) is/are *5-8*.

3. ☒ The drawings filed on *09 September 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 5-8 are allowed.

2. The following is an examiner's statement of reasons for allowance:

The primary reason for allowance is that the prior art does not teach an interconnection wiring system having the combination of a capacitor plate formed on the same layer as an interconnection wiring layer connecting underlying vias with having the capacitor formed by filling a via in an interlayer dielectric layer, where the capacitor and dielectric layer have a coplanar upper surface, as claimed.

Several references teach the general conditions of combining a capacitor with an interconnection wiring structure, such as U.S. Patent No. 5,563,762 to Leung et al. or 5,920,775 to Koh. These references do not, however, teach disposing the capacitor lower electrode in a via of the interlayer dielectric layer, such that the capacitor and dielectric layer have coplanar upper surfaces.

Although other prior art references teach disposing a capacitor lower electrode in a via, such that the electrode and surrounding dielectric layer have a coplanar upper surface, such as U.S. Patent No. 5,813,664 to Pan, there is no motivation to combine such a structure with the interconnection wiring structure in Leung or Koh, nor is there a reasonable expectation that one could change the structure or position of the capacitor of Leung or Koh without significantly changing the operability of the interconnection device. At best, such a combination would be a hindsight reconstruction of the Applicant's invention based on the Applicant's disclosure.

Since the Applicant provides specific advantages of the claimed structure, such as permitting the capacitor plates and wiring layers to be on the same level and formed from the same layer, reducing capacitive losses in the substrates, improving regularity of the capacitor plates, and eliminating debris that would result from a metal etching step to pattern the lower electrode, and since it would not be reasonable to arbitrarily combine the references discussed supra, is the Examiner's opinion that the claimed combination would not have been obvious or suggested to a person having ordinary skill in the art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Craig A. Thompson
CRAIG A. THOMPSON
PRIMARY EXAMINER